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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/031,117	01/16/2002	Takashi Kobayashi	XA-9593	3823

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EXAMINER
TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/031,117	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's Pre-amendment filed on January 16, 2002. Claims 1-46 are currently pending.

*** Claims 1, 7, 14 and 25 are objected for reciting the term "third gates" in which the modifier of "third" does not begin from a lowest order. Apparently, in light of the specification, "floating gates" should be --floating first gates--, and "control gates" should be --control second gates--.

Drawings

1. The drawings are objected to because Figure 10(c) lacks to show numeral reference "215" as described in the specification page 33, line 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-2,9-12,14-16,34-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Maruyama et al (6,034,894).

Maruyama teaches a semiconductor split type gate memory device and method thereof (at Figs 6A-6J; col 7, line 45 through col 9) comprising at least the steps of: forming a first conductivity type well in a silicon substrate (col 7, lines 50-55); forming a first pattern 13 to act as a floating gates on the silicon substrate through a first insulator film 12 (Figs 6A-6D); forming second conductivity type source/drain regions in the substrate (col 8,lines 11-17); forming a second insulator film 17 covering the first pattern 13 (Fig 6F; col 8, lines 50-56); forming third

gates 18 in gaps formed in the first pattern 13 through the second insulator film 17; forming control gates 21 (Fig 6J) on the upper surfaces of the floating gates 13 and the third gates 18, the height of the upper surface of the third gates 18 formed being lower than the height of the upper surface of the first pattern floating gates 13 (Fig 6J). Re further claims 2,16, wherein the third gate is formed by filling a polysilicon film 18' in the gaps and then dry RIE etching back (col 8, lines 50-67). Re further claims 9-10, wherein the floating gates and the third gates as erase gates are self-aligned.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 7,9-10,11-13,25,26, and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al (5,614,747) taken with Maruyama et al (6,034,894).

Ahn teaches a semiconductor split gate type flash memory device having a plurality of memory cells and method of the memory cells comprising at least the steps of: forming a first conductivity type in a silicon substrate; forming third gates 20 on the silicon substrate through a second insulator film 18 (Fig 3A); forming second conductivity type source/drain regions in the substrate; forming a first insulator film 12 (3B) covering the third gates; forming a first pattern to act as a floating gates 13 (Fig 3B) on the silicon substrate through a first insulator film 12; forming control gates 15 (Fig 3E) on the upper surfaces of the floating gates 13 and the third gates 20, the height of the upper surface of the third gates 20 formed being lower than the height

of the upper surface of the first pattern floating gates 13, wherein the floating gates and the third gates as erase gates are self-aligned.

Ahn provides the silicon substrate, but lacks forming a well in the silicon substrate.

Maruyama teaches (at col 7, lines 50-55) forming a semiconductor memory device on a silicon substrate including a well of a first conductivity.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory device of Ahn in the silicon substrate having a well of a first conductivity type as taught by Maruyama, because of the desirability to fabricate a plurality of semiconductor devices having different conductivity type in the same silicon substrate.

6. Claims 13 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al (5,614,747) and Maruyama et al (6,034,894), as applied to claims 7,9-10,11-13,25,26, and 32-38 above, taken with Ogura (5,78,341).

The references including Ahn teach a semiconductor memory device as applied above, wherein a third insulator film 14 of Ahn is silicon oxide (col 3, lines 34-36; Figs 3E).

Ahn thus lacks having a nitrogen-introduced silicon oxide.

Ogura teaches (at col 21, lines 20-30; Fig 11) forming a nitrogen-introduced silicon oxide by nitridizing of a silicon oxide.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the silicon oxide of Ahn by nitridizing to form a nitrogen-introduced silicon oxide as taught by Ogura. This is because of the desirability to minimize pin holes.

7. Claims 7-10,25-26,32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama et al (6,034,894), as applied to claims 1-2,9-12,14-16,34-38 above, taken with Takashi (JP-7-130884) or Sudo (5,555,520).

Maruyama teaches a semiconductor memory device as applied above, wherein the floating first gates 13 are firstly formed.

Maruyama thus lacks forming the third gates prior forming the floating gates.

However, Takashi alternatively teaches a first embodiment in which the third gates 17 are formed before forming the floating first gates 15 (Figs 1a-1c), and a second embodiment in

which the third gates 17 are formed after forming the floating first gates 15 (Figs 7a-7d). Sudo also teaches forming the third gates 110 before forming a second gates 114, see Figure 9 to Figure 10.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory device of Maruyama by reversing the order of steps so that the third gates are formed before forming the floating gates, as taught by Takashi or Sudo, because reversing order of steps for forming these elements would have been obvious and within the level of ordinary skill in the arts, wherein reversing order of these process steps as taught by Takashi are art recognized alternative in fabricating of semiconductor memory devices.

8. Claims 13 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama et al (6,034,894), as applied to claims 1-2,9-12,14-16,34-38 above, taken with Ogura (5,78,341).

Maruyama teaches a semiconductor memory device as applied above, wherein a third insulator film 20 includes silicon oxide (col 9, lines 5-12).

Ahn thus lacks having a nitrogen-introduced silicon oxide.

Ogura teaches (at col 21, lines 20-30; Fig 11) forming a nitrogen-introduced silicon oxide by nitridizing of a silicon oxide.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the silicon oxide of Ahn by nitridizing to form a nitrogen-introduced silicon oxide as taught by Ogura. This is because of the desirability to minimize pin holes.

9. Claims 2-6,8,17-24,27-31,40-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama et al (6,034,894) alone, or, further with Takashi (JP-7-130884) or Sudo (5,555,520), as applied to claims 7-10,25-26,32-33 above, and further of any or all of Clampitt (6,150,691), Huang (5,682,055), and Fang (6,326,293).

Maruyama teaches a semiconductor memory device as applied above, wherein the third gate is formed by filling a polysilicon conductive film 18' in the gaps and then dry RIE etching back (col 8, lines 50-67).

Maruyama thus does not list several other alternative methods including chemical mechanical polishing step for retaining a portion of the polysilicon conductive film 18' in the gaps, wherein the third gate is either completely filled or not completely filled the gaps.

However, Clampitt teaches (at Figs 5-6; col 5, lines 25-34) a method for retaining a third conductive polysilicon electrode 134 completely-filled the gaps by performing a combination of chemical mechanical polishing, wet etching, and dry etching. Clampitt also teaches (at Figs 11-15; col 5, lines 48-68) a second method for retaining a third conductive electrode 148 not-completely filled the gaps by filling the space with the photoresist film 144, and then dry etching. Huang teaches (at Figs 1A-2A; col 5, lines 1-30) chemical mechanical polishing a polysilicon film 14 with in combination with wet and dry etching, wherein a spin on glass as an silicon oxide or photoresist 24 is formed on the polysilicon film. Fang teaches (at Figs 2A-2C; col 2, line 51 through col 3) forming a conductive electrode 30 as shown in Figure 2C by chemical mechanical polishing a polysilicon film 30, then oxidizing the polysilicon surface, and selectively removing the oxidized part.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the third gates of Maruyama in the gaps by employing any other alternative methods including chemical mechanical polishing in combination with wet/dry etching as combinatively taught by Clampitt , Huang, Fang, and as well known in the art, wherein removing the oxidized part to retain a portion of the polysilicon film in the gaps is taught by Fang. This is because these methods are alternative and art recognized equivalent techniques for removing unwanted portions of the polysilicon film, wherein these alternative methods have been proven in the art to retain a portion of a polysilicon film in the gaps.

Double Patenting

10. The nonstatutory double patenting rejection or provisional rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

11. Claims 11-13 and 31-39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,438,028. Although the conflicting claims are not identical, they are not patentably distinct from each other, because the present claims 11-13 and 31-39 of this present application are anticipated and broad enough to encompass scope of claims 1-6 of the Patent No. 6,438,028.

12. Claims 1-39 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 and 79-90 of U.S. Application Serial No. 10/206,982. Although the conflicting claims are not identical, they are not patentably distinct from each other, because the present claims 1-39 of this present application are anticipated and broad enough to encompass scope of claims 1-36 and 79-90 of the Application 10/206,982.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-6

Michael Trinh
Primary Examiner